

LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising:
 - a semiconductor substrate of a first conductivity;
 - an epitaxially formed semiconductor layer of a second conductivity formed over said substrate;
 - a body region of said first conductivity formed in said epitaxially formed semiconductor layer;
 - a source region of said second conductivity formed in said body region, said source region being adjacent an invertible channel in said body region;
 - a gate structure formed over said invertible channel region, said gate structure including a gate electrode which is spaced from said invertible channel by a gate insulation layer;
 - a drain region formed in said epitaxially formed semiconductor layer, said drain region and said body region being spaced from one another by a drift region in said epitaxially formed semiconductor layer;
 - a resurf region of said first conductivity formed in said epitaxially formed semiconductor layer, said resurf region being formed over at least a portion of said drift region; and
 - a field plate structure disposed over said resurf region, said field plate structure including a first field plate disposed over a first insulation layer of a first thickness, a second field plate disposed over a second insulation layer of a second thickness, said second insulation layer being formed over said first insulation layer, and a third field plate spaced from said second field plate by a third insulation layer of a third thickness, wherein said first field plate includes a first portion spaced from a second portion by a first gap, said second field plate includes a first portion spaced from a second portion by a second gap, and said third field plate includes a first portion spaced from a second portion by a third gap, and wherein said first gap is wider than said second gap and said third gap, and said second gap is wider than said third gap, and wherein said gaps are filled only with an insulation material.

2. (Original) A semiconductor device according to claim 1, wherein said first insulation layer is comprised of an oxide.

3. (Original) A semiconductor device according to claim 1, wherein said first thickness is 0.4 microns.

4. (Original) A semiconductor device according to claim 1, wherein said second insulation layer is comprised of an oxide.

5. (Original) A semiconductor device according to claim 1, wherein said second thickness is 1.3 microns.

6. (Original) A semiconductor device according to claim 1, wherein said third insulation layer is comprised of an oxide.

7. (Original) A semiconductor device according to claim 1, wherein said third thickness is 1.4 microns.

8. (Original) A semiconductor device according to claim 1, wherein said first field plate extends from said gate electrode.

9. (Original) A semiconductor device according to claim 1, wherein said first field plate is comprised of conductive poly silicon.

10. (Canceled)

11. (Previously Presented) A semiconductor device according to claim 1, wherein said second gap is 45 microns.

12. (Canceled)

13. (Previously Presented) A semiconductor device according to claim 1, wherein said third gap is 25 microns.

14. (Previously Presented) A semiconductor device according to claim 1, wherein said first portion and said second portion of said second field plate are annular, said annular portions being disposed around said drain region.

15. (Canceled)

16. (Previously Presented) A semiconductor device according to claim 1, wherein said first portion and said second portion of said third field plate are annular, said annular portions being disposed around said drain region.

17.-19. (Canceled)

20. (Previously Presented) A semiconductor device according to claim 1, wherein said first portion of said first field plate terminates below said first portion of said second field plate.

21. (Previously Presented) A semiconductor device according to claim 1, wherein said second portion of said second field plate is electrically connected to said drain region, and to said second portion of said third field plate.

22. (Previously Presented) A semiconductor device according to claim 1, wherein said first portion of said second field plate is electrically connected to said first field plate.

23. (Previously Presented) A semiconductor device according to claim 1, wherein said first portion of said third field plate is electrically connected to said source region.

24. (Canceled)

25. (Currently Amended) A field plate structure comprising:
a first field plate;
a second field plate disposed above and spaced from said first field plate; and
a third field plate disposed above and spaced from said second field plate,
said field plate structure being disposed over a resurf region, wherein said first field plate includes a first portion spaced from a second portion by a first gap, said second field plate includes a first portion spaced from a second portion by a second gap, and said third field plate includes a first portion spaced from a second portion by a third gap, and wherein said first gap is wider than said second gap and said third gap, and said second gap is wider than said third gap, and wherein said gaps are filled only with an insulation material.

26. (Canceled)

27. (Previously Presented) A field plate structure according to claim 25, wherein said first portion and said second portion of each of said first and second field plates is annular.

28. (Previously Presented) A field plate structure according to claim 25, wherein said first portion of said second field plate is electrically connected to said first field plate and said second portion of said second field plate is electrically connected to said second portion of said third field plate.

29. (Original) A field plate structure according to claim 25, wherein said first field plate is insulated from said second field plate by an insulation layer and said second field plate is spaced from said third field plate by another insulation layer.